Wireless in
  JP4 → Signal amplifier → Volume control
  JP7 → Gain control circuit → Signal amplifier

MIC in
  JP7 → Gain control circuit → Signal amplifier

Line in
  J1 → Signal amplifier → Reverberation circuit → Tone control circuit → High-pass circuit
  JP6 → Power supply instructions and regulator circuit

Audio out to Amp
  J5 → Volume control
  J3 → Line out buffer
  J6 → Enable signal
  J10 → Boot buffer

Power supply to receiver
Filter → Amp → Filter → 110MHz Saw Filter → Amp → 10.7MHz Filter → Amp → 10.7MHz Filter → 10.7MHz Filter → FM Demodulation

PLL → VCO → 2nd Oscillator

AF-A

Noise Suppressor

10.5-16VDC IN

SUPPLY UNIT

CPU

EXP

AF-OUT

SUPPLY UNIT

CPU

AF-A
Receiver IF Scheme

Title: Receiver IF Scheme

Size: B

Date: 2006.11.23

File: LA1140A

Number: 2

Revision: 7

Drawn By:

1. Constant Voltage Circuit
2. Quadrature Limiter
3. AF Clamp
4. Mute Amp.
5. AFC
6. AGC Drive
7. Signal Level
8. Mute Drive
9. AD Level Detect
10. DC Level Detect
11. Hole Det
12. Quadrature Det
13. Level Level
14. 1st 2nd 3rd 4th 5th 6th

Symbols:
- +VRF
- GND
- R
- C
- L
- IF
- TP
- AF
- AGC
- Drive
- Mute
- Signal
- Level
- Det
- AFC
- Clamp
- DCLevel
- Inverter
- Limiter
- Quadrature
- Rssi_A
- IF_A
- LA1140A

Component Values:
- C705 102P
- R703 101
- C702 104P
- C707 103P
- R720 682
- R701 103
- C703 103p
- C709 102P
- L701 10.7MHz
- L703 10.7MHz
Receiver MCU Scheme

Title: Receiver MCU Scheme

Date: 2006.11.23

Sheet 3 of 7

Drawn By:
Amp → COMPAND → Amp → VCO BUFFER → Amp → RF

3VDC IN

SUPPLY DC/DC

ON/OFF

UP/DOWN/SET

EEPROM

32.768KHz

LCD

FILTER

PLL

SWITCHED CURREND SOURCE

Title: Bodypack Block Scheme

Size: B

Number: 1

Revision: 1

Date: 2006.11.23

File: Sheet 1 of 7

Drawn By:
HS_HT830 VCO Circuit